Claims

[c1] 1. A method for cutting a chip from a wafer, the method comprising the step of cutting around the chip along a plurality of straight-line cut segments such that all resulting corners of the chip after cutting have an angle greater than 90^{o}.

[c2] 2. The method of claim 1, wherein the angles of all the resulting corners of the chip after cutting are equal.

[c3] 3. The method of claim 1, wherein at least two consecutive straight-line cut segments of the plurality of straight-line cut segments which are not on any chip boundary line are of the same length.

[c4] 4. The method of claim 1, wherein all the straight-line cut segments of the plurality of straight-line cut segments which are not on any chip boundary line are of the same length.

[c5] 5. The method of claim 1, wherein the step of cutting around the chip along the plurality of straight-line cut segments comprises the steps of:
cutting, with a laser beam, along the straight-line cut segments of the plurality of straight-line cut segments

which are not on any chip boundary line, and cutting, with a saw blade, along the straight-line cut segments of the plurality of straight-line cut segments which are on chip boundary lines of the chip.

[c6] 6. The method of claim 1, wherein the cutting goes as deep as the entire thickness of the chip along the plurality of straight-line cut segments.

[c7] 7. The method of claim 1, wherein the cutting goes as deep as the entire thickness of the chip along the straight-line cut segments of the plurality of straight-line cut segments which are on chip boundary lines of the chip, and wherein the cutting goes only as deep as a BEOL layer along the straight-line cut segments of the plurality of straight-line cut segments which are not on any chip boundary line.

[c8] 8. The method of claim 1, wherein cutting along the straight-line cut segments of the plurality of straight-line cut segments which are not on chip boundary lines of the chip are performed with a laser beam and as deep as a BEOL layer of the chip, and wherein cutting along the straight-line cut segments of the plurality of straight-line cut segments which are on chip boundary lines of the chip are performed with a saw blade and as deep as entire the thickness of the chip.

[c9] 9. A semiconductor chip structure, comprising a plurality of straight-line cut segments around the chip such that all angles of corners of the chip are greater than 90^{o}.

[c10] 10. The chip structure of claim 9, wherein the angles of all the corners of the chip are equal.

[c11] 11. The chip structure of claim 9, wherein at least two consecutive straight-line cut segments of the plurality of straight-line cut segments which are not on chip boundary lines of the chip before dicing are of the same length.

[c12] 12. The chip structure of claim 9, further comprising a Back End of Line (BEOL) layer which comprises a low-K material.

[c13] 13. A method of dicing, comprising the steps of:providing a wafer comprising a plurality of chips sharing chip boundary lines, and
for each chip of the plurality of chips, cutting around the chip along a plurality of straight-line cut segments such that resulting corners of the chip after cutting are all greater than 90^{o}.

[c14] 14. The method of claim 13, wherein the cutting of one chip of the plurality of chips is finished before the cut-

ting of another chip of the plurality of chips is started.

[c15] 15. The method of claim 13, wherein the cutting of one chip of the plurality of chips is started before the cutting of another chip of the plurality of chips is finished.

[c16] 16. The method of claim 13, wherein the cutting is performed with a laser beam for straight-line cut segments of the plurality of straight-line cut segments which are not on any chip boundary line, and wherein the cutting is performed with a saw blade for all straight chip boundary lines comprising straight-line cut segments of the plurality of straight-line cut segments.

[c17] 17. The method of claim 13, wherein for straight-line cut segments of the plurality of straight-line cut segments which are not on chip boundary lines, the cutting is only as deep as a Back End of Line (BEOL) layer, and wherein for straight-line cut segments of the plurality of straight-line cut segments which are on chip boundary lines, the cutting is as deep as the entire thickness of the wafer.

[c18] 18. The method of claim 17, further comprising the step of cutting as deep as the entire thickness of the wafer along all the chip boundary lines.

[c19] 19. The method of claim 13, wherein the plurality of

chips are arranged in rows and columns, and wherein at least one straight chip boundary line goes through at least two straight-line cut segments of at least two chips of the plurality of chips.

[c20] 20. The method of claim 13, wherein the straight-line cut segments of the plurality of straight-line cut segments which are not on any chip boundary line of the chip are of the same length.